**AMENDMENTS TO THE DRAWINGS:**

Attached to this Amendment are replacement sheets for Figure 4 and 5.

## REMARKS

This Amendment responds to the Office Action dated September 30, 2004 in which the Examiner required a new title, objected to the drawings, rejected claims 1-4 and 11-14 under 35 U.S.C. §102(e) and rejected claims 5-10 and 15-20 under 35 U.S.C. §103.

Applicant respectfully requests the Examiner provide a new PTO 1449. In particular, on the PTO 1449 attached to the Office Action dated September 30, 2004 the references were initialed by the Examiner but the bottom of the form was not signed or dated. Applicant respectfully requests the Examiner sign and date the PTO 1449.

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As indicated above, a new title has been provided. Therefore, Applicant respectfully request the Examiner approves the new title.

Attached to this Amendment are replacement sheets for Figures 4 and 5. Applicant respectfully requests the Examiner approves the correction and withdraws the objection to the drawings.

As indicated above, the claims have been amended for stylistic reasons. The amendments are unrelated to a statutory requirement for patentability and do not narrow the literal scope of the claims.

Claim 1 claims an emulator and claim 11 claims an emulation method. The emulator and emulation method include receiving circuit design data used for implementing debugging functions, storing the circuit design data received by the receiving means and performing emulation according to the circuit design data.

Through the structure and method of the claimed invention receiving and storing circuit design data used for implementing debugging functions as claimed in claims 1 and 11, the claimed invention provides an emulator and emulation method

in which it is easy to change and update the specifications covering the debugging function without redoing the circuit design. The prior art does not show, teach or suggest the invention as claimed in claims 1 and 11.

Claims 1-4 and 11-14 were rejected under 35 U.S.C. §102(e) as being anticipated by *Tago* (U.S. Patent No. 6,598,176).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §102(e). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

*Tago* appears to disclose an apparatus for estimating (or testing) a microcontroller that has a function of executing program estimation such as program debugging, and a function of executing system estimation such as system debugging, and also relates to a method of executing program estimation and system estimation. (col. 1, lines 9-14) The estimation apparatus of the microcontroller in the basic embodiment based on the first principle includes, as shown in FIG. 3, a data holding unit 1 for holding arbitrary data rewritably, a processing unit 2 for processing the arbitrary data by operating the microcontroller on the basis of a control signal Scc, an interface unit 5 for external communication, that receives signals Sext supplied from the external, extracts the control signal Scc and sends it to the processing unit 2, and an internal bus monitoring unit 4 for monitoring the state of an internal bus 6 for connecting mutually the data holding unit 1, the processing unit 2 and the external communication interface unit 5. These constituent elements are assembled in one device (that is shown as an estimation device 9 in FIG. 3). The processing unit 2 writes the state of the internal bus 6 at the

time when the microcontroller is operated on the basis of the control signal Scc, into the internal bus monitoring unit 4 through the external communication interface unit 5, and inputs the data written into this internal bus monitoring unit 4 to the data holding unit 1 or sends it to the external. The estimation device 9 further includes a memory unit 3 for temporarily storing a program contained in the signals Sext supplied from the external. (col. 9, lines 14-36) When program estimation such as program debugging is executed in such one-chip microcontroller, the external communication interface unit 5 processes the signals Sext supplied from the external ICE, etc., takes out the control signal Scc and a program for program debugging, and transfers them to the processing unit 2 and to the memory unit 3. The processing unit 2 writes the program for debugging program into the memory unit 3, and operates the microcontroller by serially reading out the programs stored in this memory unit 3. The processing unit 2 serially writes the state of the internal bus 6 into the internal bus monitoring unit 4 while the microcontroller is being operated in this way (that is, it traces the state of the internal bus 6). The data written into the internal bus monitoring unit 4 in this way are either inputted to the data holding unit 1 through the external communication interface unit 5, or sent to the external ICE, or the like. When the content of the data held in the data holding unit 1 or the content of the data sent to the external ICE, etc., is read out, program estimation of the microcontroller such as program debugging can be executed easily. On the other hand, when the user-generated system estimation is executed in such a one-chip microcontroller, the external communication interface unit 5 processes the signals supplied from the external, takes out the control signal and the system estimation program, and transfers them to the processing unit 2. The processing unit 2 writes

the system estimation program into the data holding unit 1 on the basis of the control signal Scc while the estimation device (chip) is mounted to the estimation board. In this case, the system estimation program is written into the data holding unit 1 through the external communication interface unit 5, or through an on-board write interface (which will be explained later with reference to FIG. 5). (col. 10, lines 25-58)

Thus, *Tago* merely discloses a data hold unit 1 which stores the state of the internal bus 6 or stores a system estimation program. Nothing in *Tago* shows, teaches or suggests a receiving means for receiving circuit design data used for implementing debugging functions, a storage means for storing the circuit design data and an emulation means for performing emulation according to the circuit design data as claimed in claims 1 and 11. Rather, *Tago* merely discloses a data holding unit 1 which stores the state of an internal bus 6 (col. 9, lines 28-36, col. 10, lines 34-41) or a system estimation program (col. 10, lines 46-58).

Since nothing in *Tago* shows, teaches or suggests receiving circuit design data, storing the circuit design data and performing emulation according to the circuit design data as claimed in claims 1 and 11, Applicant respectfully requests the Examiner withdraws the rejection to claims 1 and 11 under 35 U.S.C. §102(e).

Claims 2-4 and 12-14 depend from claims 1 and 11 and recite additional features. Applicant respectfully submits that claims 2-4 and 12-14 would not have been anticipated by *Tago* within the meaning of 35 U.S.C. §102(e) at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 2-4 and 12-14 under 35 U.S.C. §102(e).

Claims 5-10 and 15-20 were rejected under 35 U.S.C. §103 as being unpatentable over *Tago* in view of *Dzoba et al.* (U.S. Patent Publication No. 2001004226).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in the primary reference to *Tago* shows, teaches or suggests the primary features as claimed in claims 1 and 11, Applicant respectfully submits that the combination of the primary reference with the secondary reference to *Dzoba et al.* will not overcome the deficiencies of the primary reference. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 5-10 and 15-20 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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Date: December 13, 2004

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